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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/362,200	07/28/1999	KAZUO NAKAZATO	2369/23	6555

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EXAMINER
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ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 07/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/362,200

Applicant(s)  
Nakazato Et.al.

Examiner  
Edgardo Ortiz

Art Unit  
2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Mar 11, 2002
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12, 15-34, 39-47, and 50-58 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12, 15-34, 39-47, and 50-58 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 13, 16 6) ☐ Other:

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### DETAILED ACTION

This Office Action is in response to an amendment filed March 11, 2002 on which Applicant amended claims 1, 3, 5, 15, 21, 35 and 45 and canceled claims 13 and 14.

#### *Priority*

1. This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a continuation of Application No. 08/958,845, filed October 28, 1997 now U.S. Patent 5,952,692." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

#### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

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A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-12, 15-34, 39-47 and 50-58 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-63 of U.S. Patent No. 5,952,692. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is readily apparent that the subject matter as taught by U.S. Patent No. 5,952,692 discloses all the limitations contained on these claims, as shown below.

With regard to Claims 1, 3, 5, 15, 21, 40, 41, 45, 50, 56, 57 and 58 of the instant application; the claims of U.S. Patent No. 5,952,692 disclose a memory device comprising a path for charge carriers, an electrode structure, a charge storage node, a lamination structure including an insulating film and a semiconductor film, the lamination, the lamination disposed between the electrode structure and the charge storing node, the lamination structure having an energy structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high an a second configuration in which the barrier

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height of the energy band profile is low, an electric current flowing in the second configuration from the electrode structure to the charge storing node and viceversa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure and wherein charge is stored on the node in the first configuration. The reference also teaches a substrate, an array of memory cells configured on the substrate, a plurality of word lines and data lines between the cells, reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually and writing circuitry to write charge onto the charge storage nodes of the cells individually.

With regard to Claims 2, 4, 6, 54, 55, the claims of U.S. Patent No. 5,952,692 disclose a memory device having a control electrode, the energy band profile being changed between the first and second configuration in response to a voltage supplied to the control electrode and controls the barrier height presented by the barrier structure to a current that flows to and from a memory node and wherein the current flows vertically through the barrier structure.

With regard to Claims 7-12, 23, 24, 42, 43, 53, the claims of U.S. Patent No. 5,952,692 disclose alternate layers of relatively electrically conductive and insulating material as part of the lamination structure or barrier layer and comprising of polysilicon and silicon nitride for the barrier structure.

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With regard to Claims 16-19, the claims of U.S. Patent No. 5,952,692 disclose a barrier structure that includes a region of barrier material providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential and wherein the height of the barrier component is raised and lowered in response to raising and lowering if the height of the barrier provided by the variable internal electrostatic barrier potential and that the barrier material is formed of a material selected from the group consisting of silicon dioxide and silicon nitride.

With regard to Claims 20, 25, 32, 33, 44, the claims of U.S. Patent No. 5,952,692 disclose a gate to receive an external bias and alter the configuration of the barrier structure.

With regard to Claim 22, the claims of U.S. Patent No. 5,952,692 disclose a source-drain path with a conductivity which is altered as a function of the charge stored on the charge storage node and the device further including a plurality of sense lines coupled to the source-drain paths of the cells and refreshing circuitry responsive to the sense lines to refresh data on the data lines.

With regard to Claims 26 and 30, the claims of U.S. Patent No. 5,952,692 disclose a charge storage node, a barrier structure that overlies the charge storage node and an electrode structure that overlies the barrier structure and that is substantially coextensive with the charge storage node.

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With regard to Claims 27-30, 46, 47 and 51, the claims of U.S. Patent No. 5,952,692 disclose source and drain regions but fails to teach an insulating layer over the substrate, comprising an oxide of the substrate and that extends over side edges of the barrier structure and the charge storage node. However, it would have been an obvious modification to someone with ordinary skill in the art, to provide an insulating layer over a substrate and comprising an oxide of the substrate, as it is a known practice in the semiconductor art and dispose said layer over side edges of the barrier structure and the charge storage node, in order to provide insulation and to use materials such as silicon for a substrate and silicon oxide or nitride for an insulating layer.

With regard to Claims 34 and 52, the claims of U.S. Patent No. 5,952,692 disclose a charge storage node but fails to teach that it comprises a conductive silicon material. However, it would have been an obvious modification to someone with ordinary skill in the art, to provide a charge storage node that comprises a conductive silicon material, as it is a known practice in the semiconductor art to use a conductive silicon material in order to store the charge carriers.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

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has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-12, 15-34, 39-47 and 50-58 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 (a) as obvious over Chen (U.S. Patent No. 5,714,766). Chen teaches on figure 9, a memory device with stacks of nanocrystals in an EEPROM-like device. The structure of Chen comprises a "lamination" structure including an insulating film (38) and a semiconductor film or dots (34). The "lamination" structure is "changeable" or "programmable" similar to applicant's claimed device. Applicant's claims are structurally and functionally anticipated or obvious over Chen. In regards to claims reciting arrays, see figures 5 and 12 of Chen.



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*Response to Arguments*

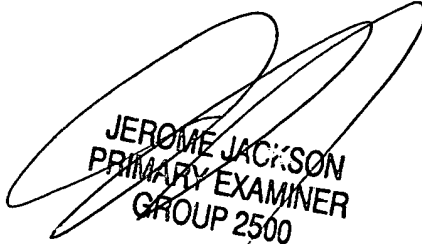
6 Applicant's arguments with respect to claims 1-12, 15-34 and 39-47 have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7724. In case the Examiner can not be reached through a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO / AU 2815

7/10/02

  
JEROME JACKSON  
PRIMARY EXAMINER  
GROUP 2500